DDR3 SDRAM Specification

240pin Unbuffered DIMM based on 1Gb E-die
64/72-bit Non-ECC/ECC

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

Table Contents

Revision History

Revision	Month	Year	History
1.0	December	2008	- First release
1.01	January	2009	- Corrected Module Physical Dimensions.
1.02	February	2009	- Added Tolerances to Physical Dimensions
1.03	July	2009	- Corrected Typo.

1.0 DDR3 Registered DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
M378B2873EH1-CF8/H9/K0	1GB	128Mx64	128Mx8(K4B1G0846E-HC##)*8	1	30mm
M391B2873EH1-CF8/H9/K0	1GB	128Mx72	128Mx8(K4B1G0846E-HC##)*9	1	30mm
M378B5673EH1-CF8/H9/K0	2GB	256Mx64	128Mx8(K4B1G0846E-HC##)*16	2	30mm
M391B5673EH1-CF8/H9/K0	2GB	256Mx72	128Mx8(K4B1G0846E-HC##)*18	2	30mm

Note :
- "##" - F8/H9/K0
- F8 - 1066Mbps 7-7-7 & H9 - 1333Mbps 9-9-9 & K0 1600Mbps 11-11-11

2.0 Key Features

Speed	DDR3-1066	DDR3-1333	DDR3-1600	Unit
	7-7-7	9-9-9	11-11-11	
tCK(min)	1.875	1.5	1.25	ns
CAS Latency	7	9	11	tCK
tRCD(min)	13.125	13.5	13.75	ns
tRP(min)	13.125	13.5	13.75	ns
tRAS(min)	37.5	36	35	ns
tRC(min)	50.625	49.5	48.75	ns

- JEDEC standard 1.5V ± 0.075V Power Supply
- V_{DDQ} = 1.5V ± 0.075V
- 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 6,7,8,9,10
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 6(DDR3-1066) and 7(DDR3-1333)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128x8(1Gb) based Module	A0-A13	A0-A9	BA0-BA2	A10/AP

4.0 x64 DIMM Pin Configurations (Front side/Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	121	V_{SS}	42	NC	162	NC	82	DQ33	202	V_{SS}
2	V_{SS}	122	DQ4	43	NC	163	V_{SS}	83	V_{SS}	203	DM4
3	DQ0	123	DQ5	44	V_{SS}	164	NC	84	$\overline{DQS4}$	204	NC
4	DQ1	124	V_{SS}	45	NC	165	NC	85	DQS4	205	V_{SS}
5	V_{SS}	125	DM0	46	NC	166	V_{SS}	86	V_{SS}	206	DQ38
6	$\overline{DQS0}$	126	NC	47	V_{SS}	167	NC (TEST)[3]	87	DQ34	207	DQ39
7	DQS0	127	V_{SS}	48	NC	168	$\overline{Reset}$	88	DQ35	208	V_{SS}
8	V_{SS}	128	DQ6	KEY				89	V_{SS}	209	DQ44
9	DQ2	129	DQ7	49	NC	169	CKE1,NC[1]	90	DQ40	210	DQ45
10	DQ3	130	V_{SS}	50	CKE0	170	V_{DD}	91	DQ41	211	V_{SS}
11	V_{SS}	131	DQ12	51	V_{DD}	171	NC	92	V_{SS}	212	DM5
12	DQ8	132	DQ13	52	BA2	172	NC	93	$\overline{DQS5}$	213	NC
13	DQ9	133	V_{SS}	53	NC	173	V_{DD}	94	DQS5	214	V_{SS}
14	V_{SS}	134	DM1	54	V_{DD}	174	A12/$\overline{BC}$	95	V_{SS}	215	DQ46
15	$\overline{DQS1}$	135	NC	55	A11	175	A9	96	DQ42	216	DQ47
16	DQS1	136	V_{SS}	56	A7	176	V_{DD}	97	DQ43	217	V_{SS}
17	V_{SS}	137	DQ14	57	V_{DD}	177	A8	98	V_{SS}	218	DQ52
18	DQ10	138	DQ15	58	A5	178	A6	99	DQ48	219	DQ53
19	DQ11	139	V_{SS}	59	A4	179	V_{DD}	100	DQ49	220	V_{SS}
20	V_{SS}	140	DQ20	60	V_{DD}	180	A3	101	V_{SS}	221	DM6
21	DQ16	141	DQ21	61	A2	181	A1	102	$\overline{DQS6}$	222	NC
22	DQ17	142	V_{SS}	62	V_{DD}	182	V_{DD}	103	DQS6	223	V_{SS}
23	V_{SS}	143	DM2	63	CK1,NC[2]	183	V_{DD}	104	V_{SS}	224	DQ54
24	$\overline{DQS2}$	144	NC	64	$\overline{CK1}$,NC[2]	184	CK0	105	DQ50	225	DQ55
25	DQS2	145	V_{SS}	65	V_{DD}	185	$\overline{CK0}$	106	DQ51	226	V_{SS}
26	V_{SS}	146	DQ22	66	V_{DD}	186	V_{DD}	107	V_{SS}	227	DQ60
27	DQ18	147	DQ23	67	V_{REF}CA	187	NC	108	DQ56	228	DQ61
28	DQ19	148	V_{SS}	68	NC	188	A0	109	DQ57	229	V_{SS}
29	V_{SS}	149	DQ28	69	V_{DD}	189	V_{DD}	110	V_{SS}	230	DM7
30	DQ24	150	DQ29	70	A10/AP	190	BA1	111	$\overline{DQS7}$	231	NC
31	DQ25	151	V_{SS}	71	BA0	191	V_{DD}	112	DQS7	232	V_{SS}
32	V_{SS}	152	DM3	72	V_{DD}	192	$\overline{RAS}$	113	V_{SS}	233	DQ62
33	$\overline{DQS3}$	153	NC	73	$\overline{WE}$	193	$\overline{S0}$	114	DQ58	234	DQ63
34	DQS3	154	V_{SS}	74	$\overline{CAS}$	194	V_{DD}	115	DQ59	235	V_{SS}
35	V_{SS}	155	DQ30	75	V_{DD}	195	ODT0	116	V_{SS}	236	V_{DDSPD}
36	DQ26	156	DQ31	76	$\overline{S1}$, NC[1]	196	A13	117	SA0	237	SA1
37	DQ27	157	V_{SS}	77	ODT1, NC[1]	197	V_{DD}	118	SCL	238	SDA
38	V_{SS}	158	NC	78	V_{DD}	198	NC	119	SA2	239	V_{SS}
39	NC	159	NC	79	NC	199	V_{SS}	120	V_{TT}	240	V_{TT}
40	NC	160	V_{SS}	80	V_{SS}	200	DQ36				
41	V_{SS}	161	NC	81	DQ32	201	DQ37				

NC = No Connect; NF = No Function; NU = Not Usable; RFU = Reserved Future Use
1. $\overline{S1}$, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs
2. CK1,NC[2] and $\overline{CK1}$,NC[2] : Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated
3. TEST (pin 167) used by memory bus analysis tools (unused on memory DIMMs)

5.0 x72 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	121	V_{SS}	42	NC	162	NC	82	DQ33	202	V_{SS}
2	V_{SS}	122	DQ4	43	NC	163	V_{SS}	83	V_{SS}	203	DM4
3	DQ0	123	DQ5	44	V_{SS}	164	CB6	84	$\overline{DQS4}$	204	NC
4	DQ1	124	V_{SS}	45	CB2	165	CB7	85	DQS4	205	V_{SS}
5	V_{SS}	125	DM0	46	CB3	166	V_{SS}	86	V_{SS}	206	DQ38
6	$\overline{DQS0}$	126	NC	47	V_{SS}	167	NC (TEST)[3]	87	DQ34	207	DQ39
7	DQS0	127	V_{SS}	48	NC	168	$\overline{Reset}$	88	DQ35	208	V_{SS}
8	V_{SS}	128	DQ6	KEY				89	V_{SS}	209	DQ44
9	DQ2	129	DQ7	49	NC	169	CKE1,NC[1]	90	DQ40	210	DQ45
10	DQ3	130	V_{SS}	50	CKE0	170	V_{DD}	91	DQ41	211	V_{SS}
11	V_{SS}	131	DQ12	51	V_{DD}	171	NC	92	V_{SS}	212	DM5
12	DQ8	132	DQ13	52	BA2	172	NC	93	$\overline{DQS5}$	213	NC
13	DQ9	133	V_{SS}	53	NC	173	V_{DD}	94	DQS5	214	V_{SS}
14	V_{SS}	134	DM1	54	V_{DD}	174	A12/$\overline{BC}$	95	V_{SS}	215	DQ46
15	$\overline{DQS1}$	135	NC	55	A11	175	A9	96	DQ42	216	DQ47
16	DQS1	136	V_{SS}	56	A7	176	V_{DD}	97	DQ43	217	V_{SS}
17	V_{SS}	137	DQ14	57	V_{DD}	177	A8	98	V_{SS}	218	DQ52
18	DQ10	138	DQ15	58	A5	178	A6	99	DQ48	219	DQ53
19	DQ11	139	V_{SS}	59	A4	179	V_{DD}	100	DQ49	220	V_{SS}
20	V_{SS}	140	DQ20	60	V_{DD}	180	A3	101	V_{SS}	221	DM6
21	DQ16	141	DQ21	61	A2	181	A1	102	$\overline{DQS6}$	222	NC
22	DQ17	142	V_{SS}	62	V_{DD}	182	V_{DD}	103	DQS6	223	V_{SS}
23	V_{SS}	143	DM2	63	CK1,NC[2]	183	V_{DD}	104	V_{SS}	224	DQ54
24	$\overline{DQS2}$	144	NC	64	$\overline{CK1}$,NC[2]	184	CK0	105	DQ50	225	DQ55
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26	V_{SS}	146	DQ22	66	V_{DD}	186	V_{DD}	107	V_{SS}	227	DQ60
27	DQ18	147	DQ23	67	$V_{REF}CA$	187	$\overline{EVENT}$	108	DQ56	228	DQ61
28	DQ19	148	V_{SS}	68	NC	188	A0	109	DQ57	229	V_{SS}
29	V_{SS}	149	DQ28	69	V_{DD}	189	V_{DD}	110	V_{SS}	230	DM7
30	DQ24	150	DQ29	70	A10/AP	190	BA1	111	$\overline{DQS7}$	231	NC
31	DQ25	151	V_{SS}	71	BA0	191	V_{DD}	112	DQS7	232	V_{SS}
32	V_{SS}	152	DM3	72	V_{DD}	192	$\overline{RAS}$	113	V_{SS}	233	DQ62
33	$\overline{DQS3}$	153	NC	73	$\overline{WE}$	193	$\overline{S0}$	114	DQ58	234	DQ63
34	DQS3	154	V_{SS}	74	$\overline{CAS}$	194	V_{DD}	115	DQ59	235	V_{SS}
35	V_{SS}	155	DQ30	75	V_{DD}	195	ODT0	116	V_{SS}	236	V_{DDSPD}
36	DQ26	156	DQ31	76	$\overline{S1}$, NC[1]	196	A13	117	SA0	237	SA1
37	DQ27	157	V_{SS}	77	ODT1, NC[1]	197	V_{DD}	118	SCL	238	SDA
38	V_{SS}	158	CB4	78	V_{DD}	198	NC	119	SA2	239	V_{SS}
39	CB0	159	CB5	79	NC	199	V_{SS}	120	V_{TT}	240	V_{TT}
40	CB1	160	V_{SS}	80	V_{SS}	200	DQ36				
41	V_{SS}	161	DM8	81	DQ32	201	DQ37				

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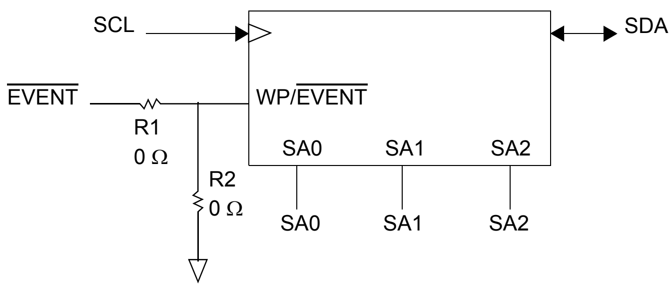
6.0 Pin Description

Pin Name	Description	Pin Name	Description
A0-A13	SDRAM address bus	SCL	I^2C serial bus clock for EEPROM
BA0-BA2	SDRAM bank select	SDA	I^2C serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0-SA2	I^2C serial address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}*	SDRAM core power supply
$\overline{WE}$	SDRAM write enable	V_{DDQ}*	SDRAM I/O Driver power supply
$\overline{S0}$, $\overline{S1}$	DIMM Rank Select Lines	V_{REFDQ}	SDRAM I/O reference supply
CKE0,CKE1	SDRAM clock enable lines	V_{REFCA}	SDRAM command/address reference supply
ODT0, ODT1	On-die termination control lines	V_{SS}	Power supply return (ground)
DQ0 - DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
CB0 - CB7	DIMM ECC check bits	NC	Spare Pins(no connect)
DQS0 - DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
$\overline{DQS0}$-$\overline{DQS8}$	SDRAM differential data strobes (negative line of differential pair)	$\overline{RESET}$	Set DRAMs Known State
DM0-DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	$\overline{EVENT}$	Reserved for optional temperature-sensing hardware
CK0, CK1	SDRAM clocks (positive line of differential pair)	V_{TT}	SDRAM I/O termination supply
$\overline{CK0}$, $\overline{CK1}$	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

*The V_{DD} and V_{DDQ} pins are tied common to a single power-plane on these designs.

7.0 SPD and Thermal Sensor for ECC UDIMMs

On DIMM thermal sensor will provide DRAM temperature readout through a integrated thermal sensor.



Note :

1. Raw Cards D (1Rx8 ECC) and E (2Rx8 ECC) support a thermal sensor.
2. When the SPD and the thermal sensor are placed on the module, R1 is placed but R2 is not.
   When only the SPD is placed on the module, R2 is placed but R1 is not.

Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	Notes
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

8.0 Input/Output Functional Description

Symbol	Type	Function
CK0-CK1 $\overline{\text{CK0}}$-$\overline{\text{CK1}}$	SSTL	CK and $\overline{\text{CK}}$ are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is reference to the crossing of CK and $\overline{\text{CK}}$ (Both directions of crossing)
CKE0-CKE1	SSTL	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self-Refresh mode
$\overline{\text{S0}}$-$\overline{\text{S1}}$	SSTL	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	SSTL	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ (ALONG WITH $\overline{\text{S}}$) define the command being entered.
ODT0-ODT1	SSTL	When high, termination resistance is enabled for all DQ, DQS, $\overline{\text{DQS}}$ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
V_{REFDQ}	Supply	Reference voltage for SSTL 15 I/O inputs.
V_{REFCA}	Supply	Reference voltage for SSTL 15 command/address inputs.
V_{DDQ}	Supply	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA0-BA2	SSTL	Selects which SDRAM bank of eight is activated.
A0-A13	SSTL	During a Bank Activate command cycle, Address input defines the row address (RA0-RA13) During a Read or Write command cycle, Address input defines the column address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a pre-charge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12($\overline{\text{BC}}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; Low, burst chopped).
DQ0-DQ63 CB0-CB7	SSTL	Data and Check Bit Input/Output pins.
DM0-DM8	SSTL	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply	Power and ground for DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS0-DQS8 $\overline{\text{DQS0}}$-$\overline{\text{DQS8}}$	SSTL	Data strobe for input and output data. For raw cards using x16 organized DRAMs, Pins DQ0-7 are associated with the LDQS and $\overline{\text{LDQS}}$ pins and Pins DQ8-15 are associated with UDQS and $\overline{\text{UDQS}}$ pins.
SA0-SA2	-	These signals and tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EERPOM address range.
SDA	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pull-up on the system board.
SCL	-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V_{DDSPD} to act as a pull-up on the system board.
V_{DDSPD}	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 3.0V to 3.6V.
$\overline{\text{RESET}}$	-	The $\overline{\text{RESET}}$ pin is connected to the $\overline{\text{RESET}}$ pin on each DRAM. When low, all DRAMs are set to a know state.
$\overline{\text{EVENT}}$	Output	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the $\overline{\text{EVENT}}$ pin on TS/SPD part

8.1 Address Mirroring Feature

There is a via grid located under the DRAMs for wiring the CA signals (address, bank address, command, and control lines) to the DRAM pins. The length of the traces from the vias to the DRAMs places limitations on the bandwidth of the module. The shorter these traces, the higher the bandwidth. To extend the bandwidth of the CA bus for DDR3 modules, a scheme was defined to reduce the length of these traces.
The pins on the DRAM are defined in a manner that allows for these short trace lengths. The CA bus pins in Columns 2 and 8, ignoring the mechanical support pins, do not have any special functions (secondary functions). This allows the most flexibility with these pins. These are address pins A3, A4, A5, A6, A7, A8 and bank address pins BA0 and BA1. Refer to Table . Rank 0 DRAM pins are wired straight, with no mismatch between the connector pin assignment and the DRAM pin assignment. Some of the Rank 1 DRAM pins are cross wired as defined in the table. Pins not listed in the table are wired straight.

8.1.1 DRAM Pin Wiring Mirroring

Connector Pin	DRAM Pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

Figure 1 illustrates the wiring in both the mirrored and non-mirrored case. The lengths of the traces to the DRAM pins, is obviously shorter. The via grid is smaller as well.

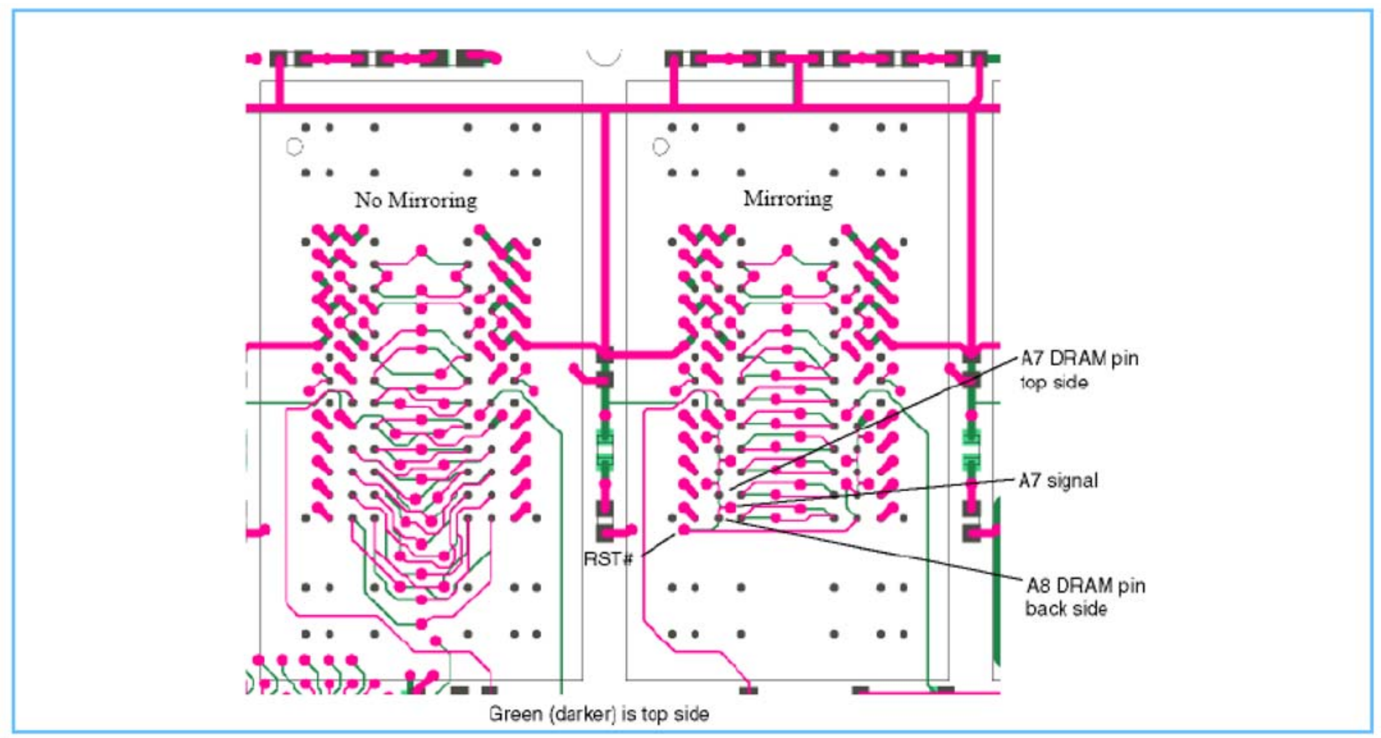
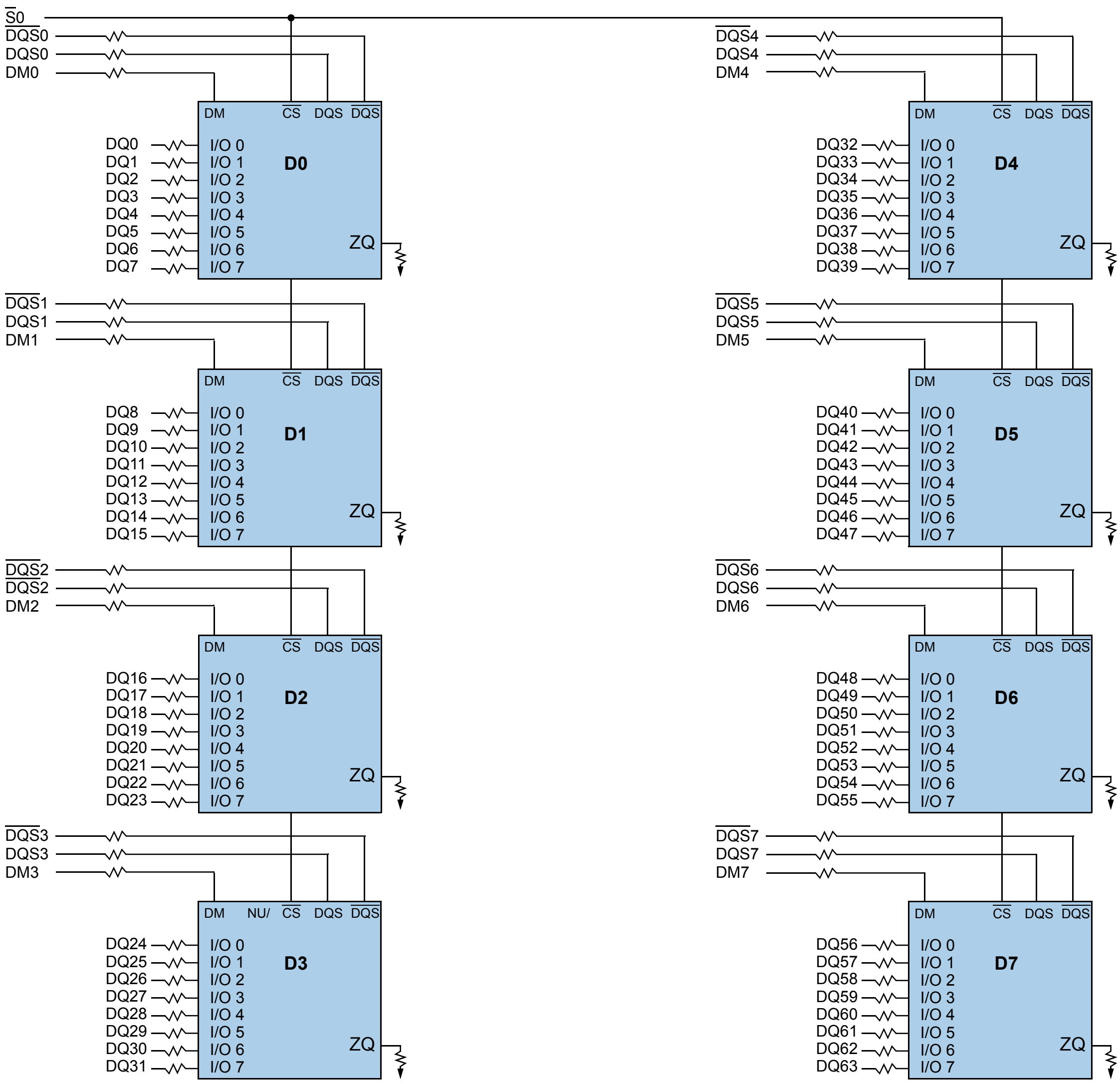


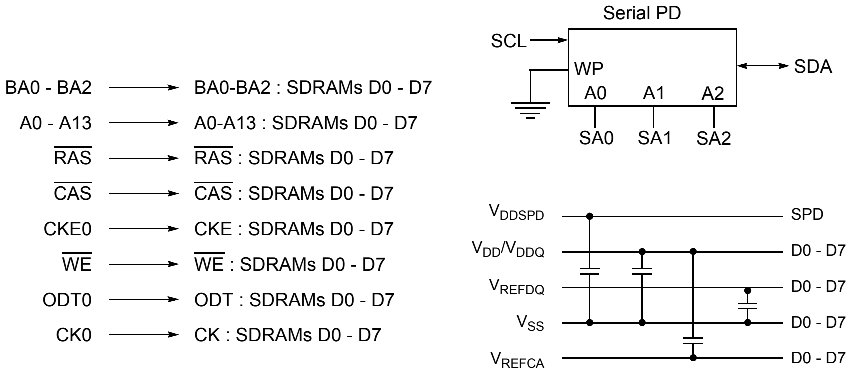
Figure 1. Wiring Differences for Mirrored and Non-Mirrored Addresses

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. This requires a few rules. Mirroring is done on 2 rank modules and can only be done on the second rank. There is not a requirement that the second rank be mirrored. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR3 UDIMM SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the second rank.

9.0 Function Block Diagram:

9.1 1GB, 128Mx64 Module (Populated as 1 rank of x8 DDR3 SDRAMs)

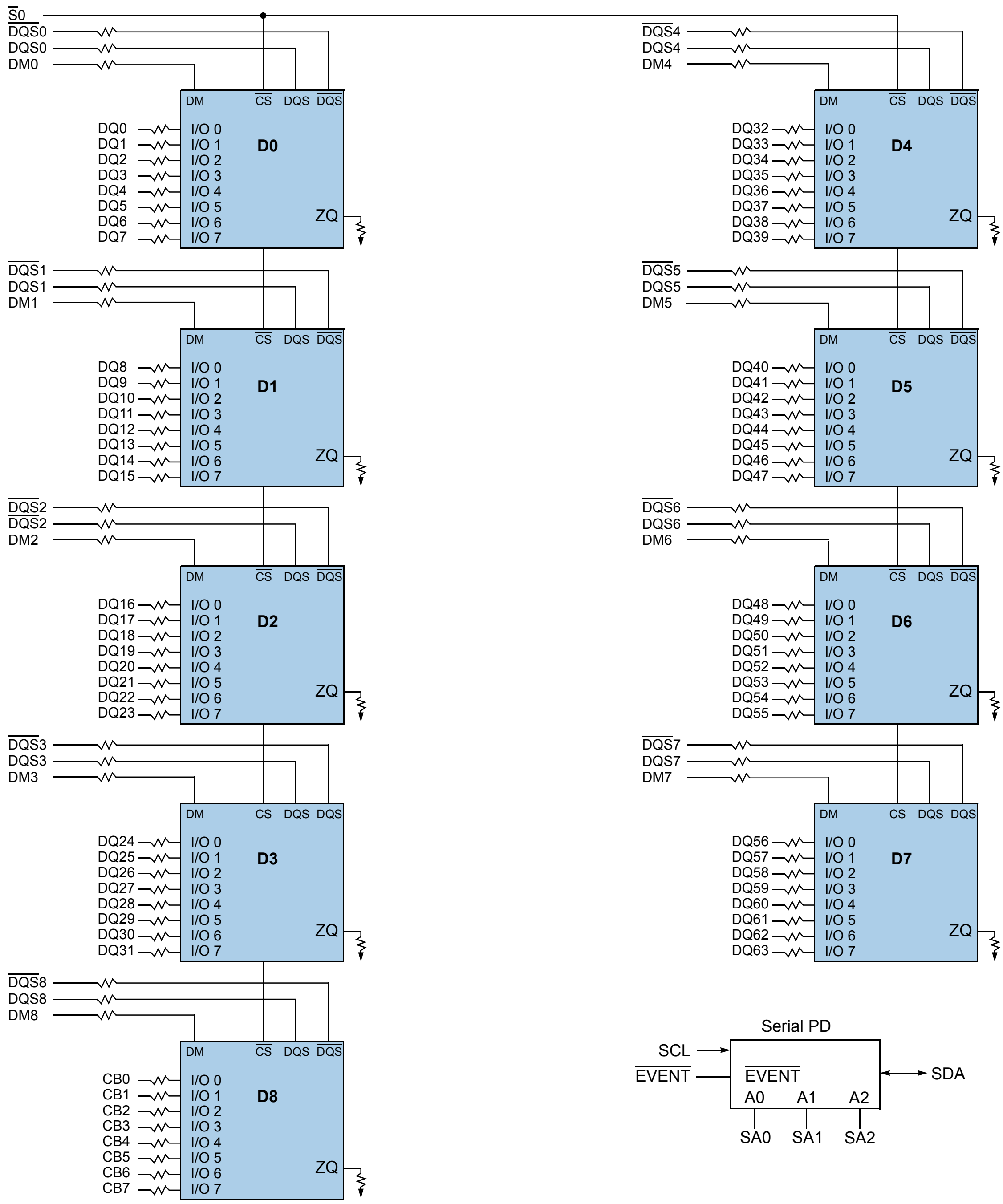




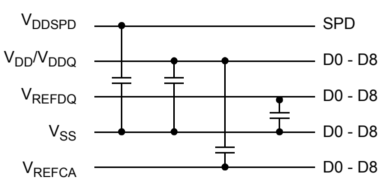
Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ, DM, DQS/DQS resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
5. Refer to section 7.1 of this document for details on address mirroring.
6. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
7. One SPD exists per module.

9.2 1GB, 128Mx72 Module (Populated as 1 rank of x8 DDR3 SDRAMs)



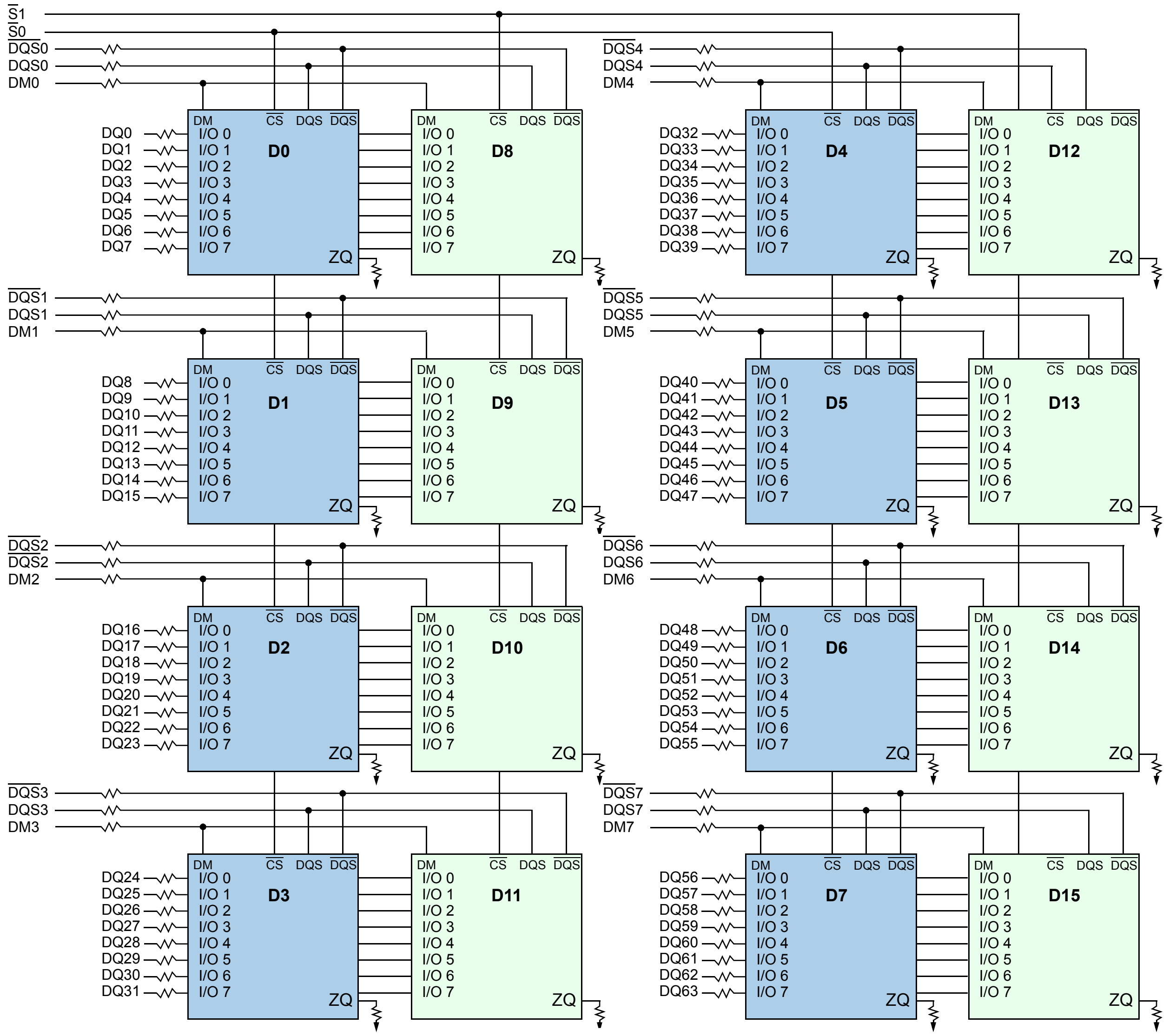
BA0 - BA2	→	BA0-BA2 : SDRAMs D0 - D8
A0 - A15	→	A0-A15 : SDRAMs D0 - D8
RAS	→	RAS : SDRAMs D0 - D8
CAS	→	CAS : SDRAMs D0 - D8
CKE0	→	CKE : SDRAMs D0 - D8
WE	→	WE : SDRAMs D0 - D8
ODT0	→	ODT : SDRAMs D0 - D8
CK0	→	CK : SDRAMs D0 - D8



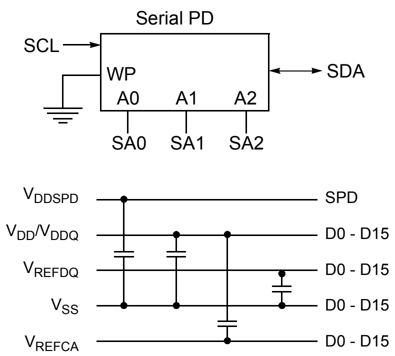
Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ, CB, DM, DQS/DQS resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
5. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
6. Refer to "SPD and Thermal sensor for ECC UDIMMs" for SPD detail.

9.3 2GB, 256Mx64 Module (Populated as 2 ranks of x8 DDR3 SDRAMs)



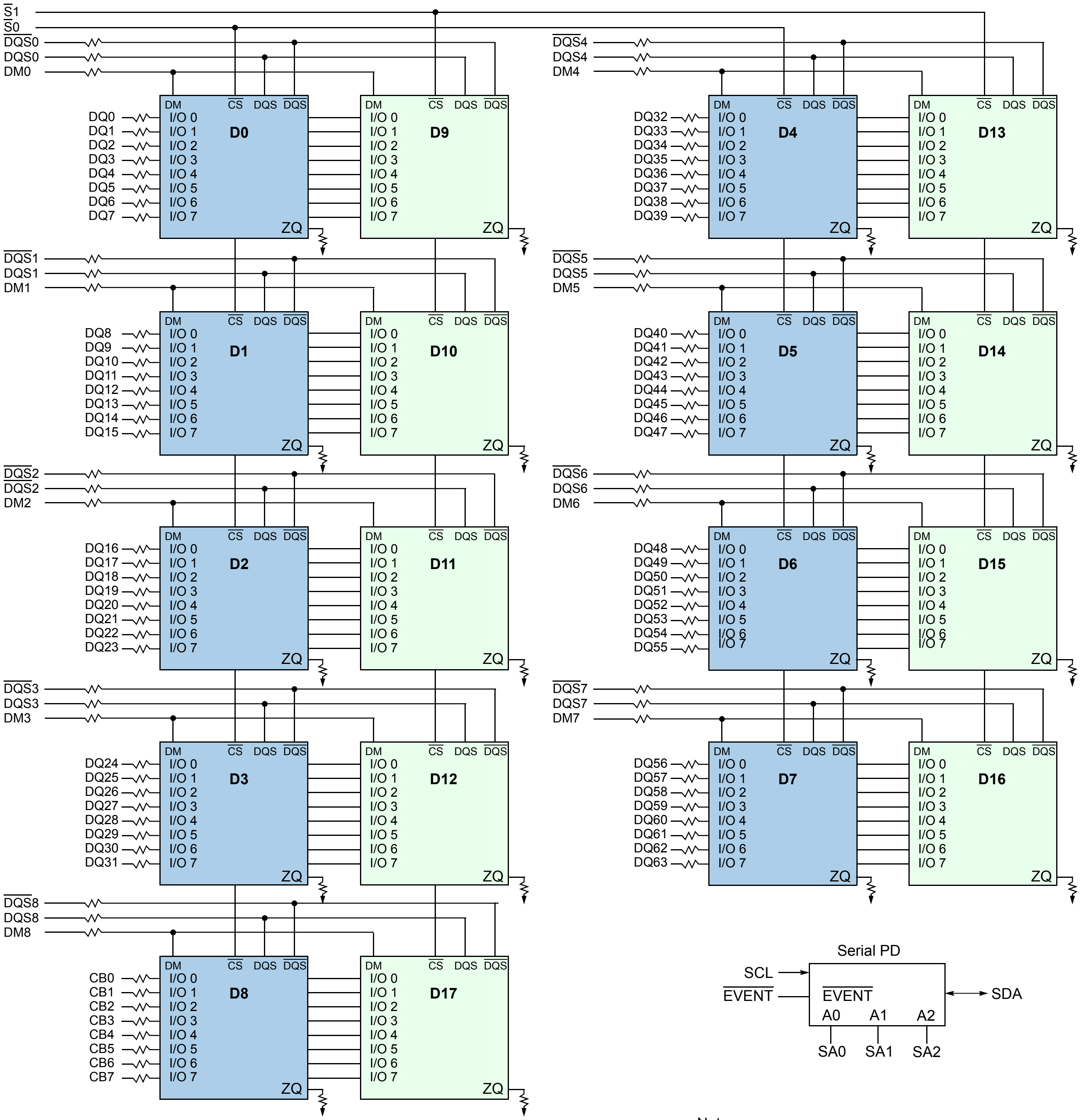
- BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D15
- A0 - A15 → A0-A15 : SDRAMs D0 - D15
- CKE1 → CKE : SDRAMs D8 - D15
- CKE0 → CKE : SDRAMs D0 - D7
- $\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D15
- $\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D15
- $\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D15
- ODT0 → ODT : SDRAMs D0 - D7
- ODT1 → ODT : SDRAMs D8 - D15
- CK0 → CK : SDRAMs D0 - D7
- CK1 → CK : SDRAMs D8 - D15



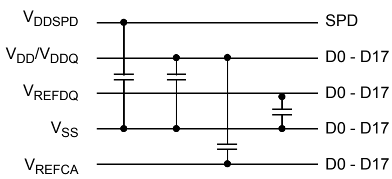
Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationships must be maintained as shown.
3. DQ, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to section 7.1 of this document for details on address mirroring.
5. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
6. One SPD exists per module.

9.4 2GB, 256Mx72 ECC Module (Populated as 2 ranks of x8 DDR3 SDRAMs)



BA0 - BA2	→	BA0-BA2 : SDRAMs D0 - D17
A0 - A15	→	A0-A15 : SDRAMs D0 - D17
CKE1	→	CKE : SDRAMs D9 - D17
CKE0	→	CKE : SDRAMs D0 - D8
RAS	→	RAS : SDRAMs D0 - D17
CAS	→	CAS : SDRAMs D0 - D17
WE	→	WE : SDRAMs D0 - D17
ODT0	→	ODT : SDRAMs D0 - D8
ODT1	→	ODT : SDRAMs D9 - D17
CK0	→	CK : SDRAMs D0 - D8
CK1	→	CK : SDRAMs D9 - D17



Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ, CB, DM, DQS, DQS resistors: Refer to associated topology diagram.
4. Refer to section 7.1 of this document for details on address mirroring.
5. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
6. Refer to "SPD and Thermal sensor for ECC UDIMMs" for SPD detail.

10.0 Absolute Maximum Ratings

10.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times;and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

10.2 DRAM Component Operating Temperature Range

Symbol	Parameter	rating	Unit	Notes
T_{OPER}	Operating Temperature Range	0 to 95	°C	1, 2, 3

Note :
1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b)

11.0 AC & DC Operating Conditions

11.1 Recommended DC Operating Conditions (SSTL - 15)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

Note :
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

12.0 AC & DC Input Measurement Levels

12.1 AC & DC Logic Input Levels for Single-ended Signals

Single Ended AC and DC input levels for Command and Address

Symbol	Parameter	DDR3-1066		DDR3-1333		Unit	Notes
		Min.	Max.	Min.	Max.		
$V_{IH.CA}$(DC)	DC input logic high	V_{REF} + 100	V_{DD}	V_{REF} + 100	V_{DD}	mV	1
$V_{IL.CA}$(DC)	DC input logic low	V_{SS}	V_{REF} - 100	V_{SS}	V_{REF} - 100	mV	1
$V_{IH.CA}$(AC)	AC input logic high	V_{REF} + 175	-	V_{REF} + 175	-	mV	1,2
$V_{IL.CA}$(AC)	AC input logic low	-	V_{REF} - 175	-	V_{REF} - 175	mV	1,2
$V_{IH.CA}$(AC150)	AC input logic high	-	-	V_{REF}+150	-	mV	1,2
$V_{IL.CA}$(AC150)	AC input logic low	-	-	-	V_{REF}-150	mV	1,2
V_{REFCA}(DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	0.49*V_{DD}	0.51*V_{DD}	V	3,4

Note :
1. For input only pins except $\overline{RESET}$, V_{REF} = V_{REFCA}(DC)
2. See "Overshoot and Undershoot specifications" section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than ± 1% V_{DD} (for reference : approx. ± 15mV)
4. For reference : approx. V_{DD}/2 ± 15mV

Single Ended AC and DC input levels for DQ and DM

Symbol	Parameter	DDR3-1066		DDR3-1333/1600		Unit	Notes
		Min.	Max.	Min.	Max.		
$V_{IH.DQ}$(DC100)	DC input logic high	V_{REF} + 100	V_{DD}	V_{REF} + 100	V_{DD}	mV	1
$V_{IL.DQ}$(DC100)	DC input logic low	V_{SS}	V_{REF} - 100	V_{SS}	V_{REF} - 100	mV	1
$V_{IH.DQ}$(AC175)	AC input logic high	V_{REF} + 175	-	V_{REF} + 150	-	mV	1,2,5
$V_{IL.DQ}$(AC175)	AC input logic low	-	V_{REF} - 175	-	V_{REF} - 150	mV	1,2,5
$V_{IH.DQ}$(AC150)	AC input logic high	V_{REF} + 150	Note 2	-	-	mV	1,2,5
$V_{IL.DQ}$(AC150)	AC input logic low	Note 2	V_{REF} - 150	-	-	mV	1,2,5
V_{REFDQ}(DC)	I/O Reference Voltage(DQ)	0.49*V_{DD}	0.51*V_{DD}	0.49*V_{DD}	0.51*V_{DD}	V	3,4

Note :
1. For input only pins except $\overline{RESET}$, V_{REF} = V_{REFDQ}(DC)
2. See 9.6 "Overshoot and Undershoot specifications" section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than ± 1% V_{DD} (for reference : approx. ± 15mV)
4. For reference : approx. V_{DD}/2 ± 15mV
5. Single ended swing requirement for DQS - $\overline{DQS}$ is 350mV (peak to peak). Differential swing for DQS - $\overline{DQS}$ is 700mV (peak to peak).

12.2 V_{REF} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in Figure 2. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements of V_{REF}. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than ± 1% V_{DD}.

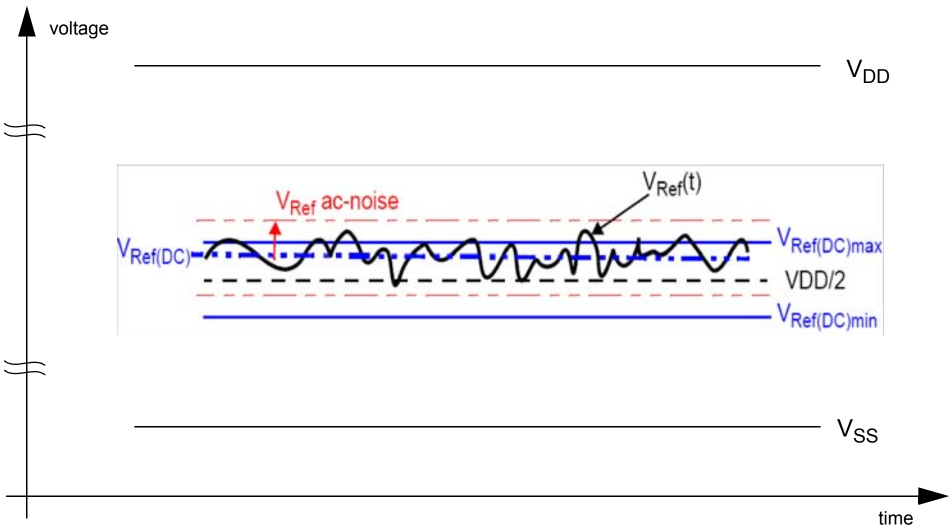


Figure 2. Illustration of $V_{REF}(DC)$ tolerance and V_{REF} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF}.

"V_{REF}" shall be understood as $V_{REF}(DC)$, as defined in Figure 2.

This clarifies, that dc-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} ac-noise. Timing and voltage effects due to ac-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

12.3 AC & DC Logic Input Levels for Differential Signals

12.3.1 Differential Signals Definition

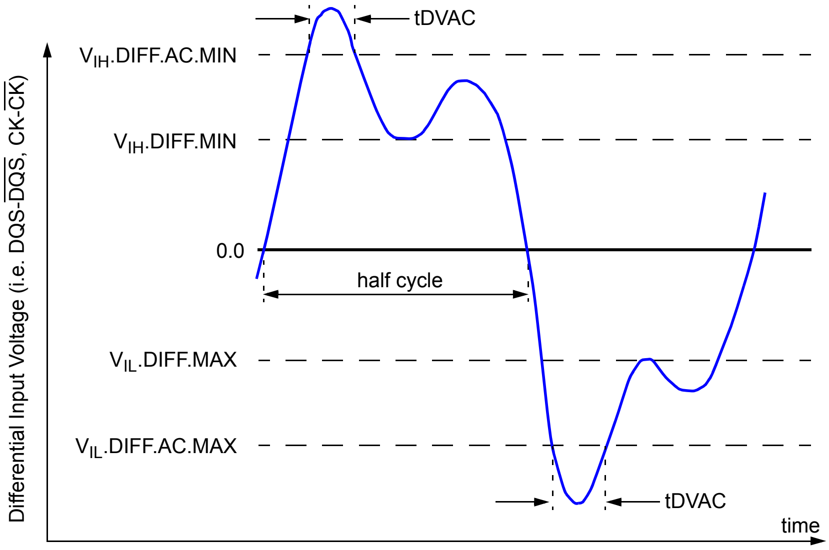


Figure 3. Definition of differential ac-swing and "time above ac level" tDVAC

12.3.2 Differential Swing Requirement for Clock (CK - $\overline{CK}$) and Strobe (DQS - $\overline{DQS}$)

Symbol	Parameter	DDR3-1066/1333		unit	Note
		min	max		
V_{IHdiff}	differential input high	+0.2	note 3	V	1
V_{ILdiff}	differential input low	note 3	-0.2	V	1
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC)-V_{REF})	note 3	V	2
V_{ILdiff}(AC)	differential input low ac	note 3	2 x (V_{REF} - V_{IL}(AC))	V	2

Notes:
1. Used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use V_{IH}/V_{IL}(AC) of ADD/CMD and V_{REFCA}; for DQS - $\overline{DQS}$, DQSL - $\overline{DQSL}$, DQSU - $\overline{DQSU}$ use V_{IH}/V_{IL}(AC) of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "overshoot and Undersheet Specification " on page20.

Allowed time before ringback (tDVAC) for CLK - $\overline{CLK}$ and DQS - $\overline{DQS}$.

Slew Rate [V/ns]	tDVAC [ps] @ $\lvert V_{IH/Ldiff}(AC)\rvert$ = 350mV		tDVAC [ps] @ $\lvert V_{IH/Ldiff}(AC)\rvert$ = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

12.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, or $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.
CK and $\overline{CK}$ have to approximately reach V_{SEH}min / V_{SEL}max (approximately equal to the ac-levels (V_{IH}(AC) / V_{IL}(AC)) for ADD/CMD signals) in every half-cycle.
DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach V_{SEH}min / V_{SEL}max (approximately the ac-levels (V_{IH}(AC) / V_{IL}(AC)) for DQ signals) in every half-cycle proceeding and following a valid transition.
Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if V_{IH}150(AC)/V_{IL}150(AC) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.

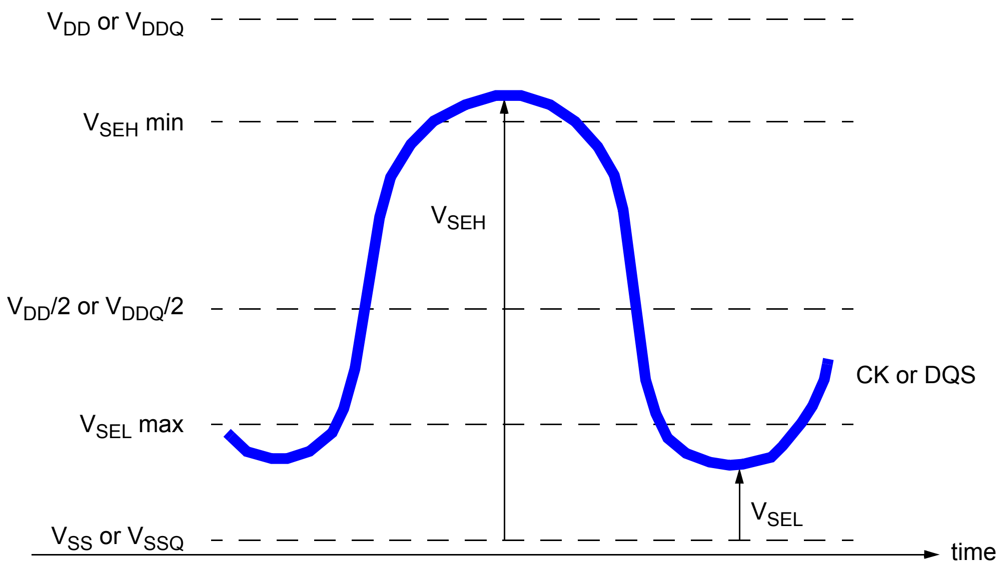


Figure 4. Single-ended requirement for differential signals

Note that while ADD/CMD and DQ signal requirements are with respect to V_{REF}, the single-ended components of differential signals have a requirement with respect to V_{DD}/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}max, V_{SEH}min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

Symbol	Parameter	DDR3-1066/1333		Unit	Notes
		Min	Max		
V_{SEH}	Single-ended high-level for strobes	(V_{DD}/2)+0.175	Note3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	(V_{DD}/2)+0.175	Note3	V	1, 2
V_{SEL}	Single-ended low-level for strobes	Note3	(V_{DD}/2)-0.175	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	Note3	(V_{DD}/2)-0.175	V	1, 2

Notes:
1. For CK, $\overline{CK}$ use V_{IH}/V_{IL}(AC) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use V_{IH}/V_{IL}(AC) of DQs.
2. V_{IH}(AC)/V_{IL}(AC) for DQs is based on V_{REFDQ}; V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specification"

12.3.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signal to the mid level between of V_{DD} and V_{SS}.

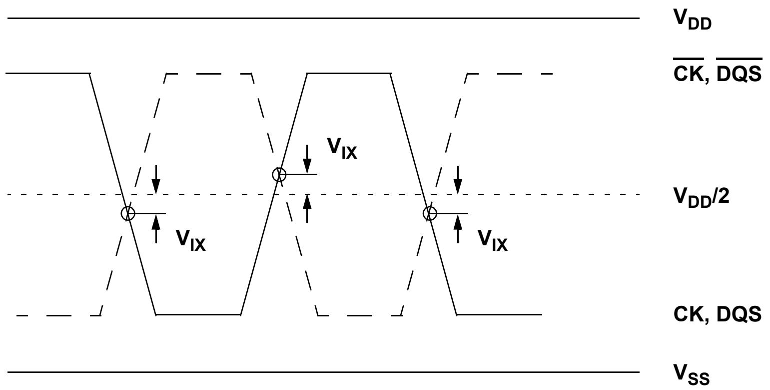


Figure 5. V_{IX} Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-1066/1333		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK,$\overline{CK}$	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS,$\overline{DQS}$	-150	150	mV	

Note :
1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic, have a single-ended swing V_{SEL} / V_{SEH} of at least $V_{DD}/2$ =/-250 mV, and the differential slew rate of CK-$\overline{CK}$ is larger than 3 V/ ns. Refer to table 11 on page 17 for V_{SEL} and V_{SEH} standard values.

12.4 Slew Rate Definition for Single-ended Input Signals

See "Address / Command Setup, Hold and Derating" for single-ended slew rate definitions for address and command signals.
See "Data Setup, Hold and Slew Rate Derating" for single-ended slew rate definitions for data signals.tDH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(DC)min and the first crossing of V_{REF}

12.5 Slew Rate Definition for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in below.

Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$\frac{V_{IHdiffmin} - V_{ILdiffmax}}{\text{Delta TRdiff}}$
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$\frac{V_{IHdiffmin} - V_{ILdiffmax}}{\text{Delta TFdiff}}$

Note : The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds

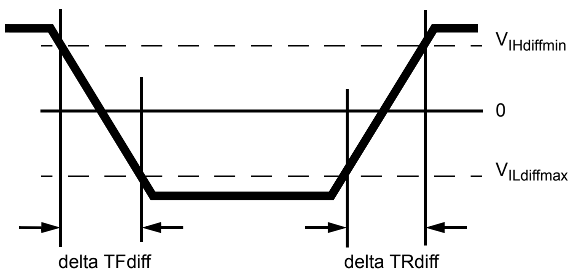


Figure 6. Differential Input Slew Rate definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

13.0 AC & DC Output Measurement Levels

13.1 Single-ended AC & DC Output Levels

Single Ended AC and DC output levels

Symbol	Parameter	DDR3-1066/1333	Units	Notes
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Note : 1. The swing of +/-0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT}=V_{DDQ}/2.

13.2 Differential AC & DC Output Levels

Differential AC and DC output levels

Symbol	Parameter	DDR3-1066/1333	Units	Notes
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.2 x V_{DDQ}	V	1
V_{OLdiff}(DC)	AC differential output low measurement level (for output SR)	-0.2 x V_{DDQ}	V	1

Note : 1. The swing of +/-0.2xV_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT}=V_{DDQ}/2 at each of the differential outputs.

13.3 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC) for single ended signals as shown in below.

Single Ended Output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	$\frac{V_{OH}(AC)-V_{OL}(AC)}{\text{Delta TRse}}$
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	$\frac{V_{OH}(AC)-V_{OL}(AC)}{\text{Delta TFse}}$

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.

Single Ended Output slew rate

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	2.5	5	2.5	5	TBD	5	V/ns

Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output
se : Singe-ended Signals
For Ron = RZQ/7 setting

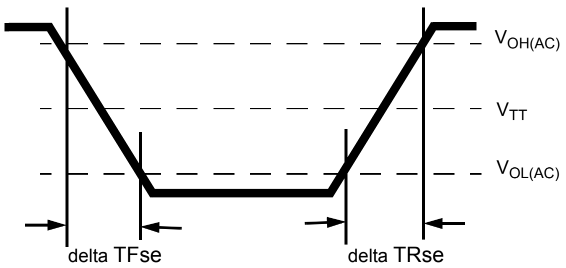


Figure 7. Single Ended Output Slew Rate definition

13.4 DIfferential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OLdiff}(AC) and V_{OHdiff}(AC) for differential signals as shown in below.

Differential Output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}(AC)	V_{OHdiff}(AC)	$\frac{V_{OHdiff}(AC)-V_{OLdiff}(AC)}{\text{Delta TRdiff}}$
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	$\frac{V_{OHdiff}(AC)-V_{OLdiff}(AC)}{\text{Delta TFdiff}}$

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.

Differential Output slew rate

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQse	5	10	5	10	TBD	10	V/ns

Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output
diff : Singe-ended Signals

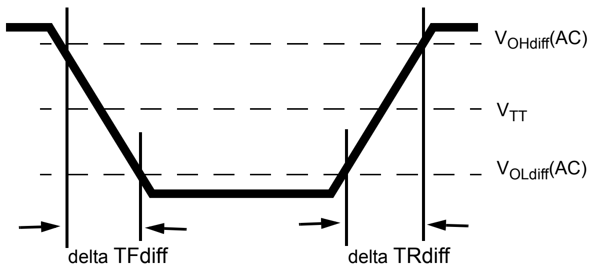


Figure 8. Differential Output Slew Rate definition

14.0 IDD Specification Definition

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL:** see Table 30 ; **BL**: 8[a]; **AL**: 0; $\overline{CS}$: High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling according to Table 32 ; **Data IO:** MID-LEVEL; **DM:**stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table32); **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 32
IDD1	**Operating One Bank Active-Read-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL:** see Table 30 ; **BL**: 8[a]; **AL**: 0; $\overline{CS}$: High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling according to Table 33 ; **DM:**stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table33); **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 33
IDD2N	**Precharge Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 34 ; **Data IO:** MID-LEVEL; **DM:**stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 34
DD2NT	**Precharge Standby ODT Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 35 ; **Data IO:** MID-LEVEL;**DM:**stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** toggling according to Table 35 ; **Pattern Details:** see Table 35
DDQ2NT (optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2P0	**Precharge Power-Down Current Slow Exit** **CKE:** Low; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:**stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pecharge Power Down Mode:** Slow Exi[c]
IDD2P1	**Precharge Power-Down Current Fast Exit** **CKE:** Low; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:**stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pecharge Power Down Mode:** Fast Exit[c]
IDD2Q	**Precharge Quiet Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:**stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 34 ; **Data IO:** MID-LEVEL; **DM:**stable at 0;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 34
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: High between RD; **Command, Address, Bank Address Inputs:** partially toggling according to Table 36 ; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 36 ; **DM:**stable at 0; **Bank Activity:** all banks open, **RD commands cycling through banks:** 0,0,1,1,2,2,... (see Table 7 on page 10); **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 36
IDDQ4R (optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: High between WR; **Command, Address, Bank Address Inputs:** partially toggling according to Table 37 ; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 37; **DM:** stable at 0; **Bank Activity:** all banks open, **WR commands cycling through banks:** 0,0,1,1,2,2,... (see Table 37); **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 37
IDD5B	**Burst Refresh Current** **CKE:** High; **External clock:** On; **tCK, CL, nRFC:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$: High between REF; **Command, Address, Bank Address Inputs:** partially toggling according to Table 38 ; **Data IO:** MID-LEVEL;**DM:**stable at 0; **Bank Activity:** REF command every nRFC (see Table 38); **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 38
IDD6	**Self Refresh Current: Normal Temperature Range** **TCASE:** 0 - 85°C; **Auto Self-Refresh (ASR):** Disabled[d]; **Self-Refresh Temperature Range (SRT): N**ormal[e]; **CKE:** Low; **External clock:** Off; **CK and** $\overline{\textbf{CK}}$**:** LOW; **CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{CS}$, Command, Address, Bank Address, **Data IO:** MID-LEVEL;**DM:**stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** MID-LEVEL

Symbol	Description
IDD6ET	**Self-Refresh Current: Extended Temperature Range (optional)[f]** **TCASE:** 0 - 95°C; **Auto Self-Refresh (ASR):** Disabled[d]; **Self-Refresh Temperature Range (SRT):** Extended[e]; CKE: Low; **External clock:** Off; **CK and $\overline{\text{CK}}$:** LOW; **CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{\text{CS}}$, Command, Address, Bank Address, **Data IO:** MID-LEVEL;**DM:**stable at 0; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** MID-LEVEL
IDD6TC	**Auto Self-Refresh Current (optional)[f]** **TCASE:** 0 - 95°C; **Auto Self-Refresh (ASR):** Enabled[d]; **Self-Refresh Temperature Range (SRT):** Normal[e]; **CKE:** Low; **External clock:** Off; **CK and $\overline{\text{CK}}$**: LOW; **CL:** see Table 30 ; **BL:** 8[a]; **AL:** 0; $\overline{\text{CS}}$, Command, Address, Bank Address, **Data IO:** MID-LEVEL; **DM:**stable at 0; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** MID-LEVEL
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, **CL:** see Table 30 ; **BL:** 8[a, g]; **AL:** CL-1; $\overline{\text{CS}}$: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling according to Table 39 ; **Data IO:** read data bursts with different data between one burst and the next one according to Table 39 ; **DM:**stable at 0; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 39 ; **Output Buffer and RTT:** Enabled in Mode Registers[b]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 39

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
c) Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
e) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
f) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device
g) IDD current measure method and detail patterns are described on DDR3 component datasheet

14.1 IDD SPEC Table

M378B2873EH1 : 1GB(128Mx64) Module

Symbol	CF8 (DDR3-1066@CL=7)	CH9 (DDR3-1333@CL=9)	CK0 (DDR3-1600@CL=11)	Unit	Notes
IDD0	480	520	TBD	mA	
IDD1	600	640	TBD	mA	
IDD2P0(slow exit)	80	80	TBD	mA	
IDD2P1(fast exit)	200	200	TBD	mA	
IDD2N	240	280	TBD	mA	
IDD2Q	240	280	TBD	mA	
IDD3P(fast exit)	200	200	TBD	mA	
IDD3N	360	400	TBD	mA	
IDD4R	840	1000	TBD	mA	
IDD4W	920	1080	TBD	mA	
IDD5B	1200	1280	TBD	mA	
IDD6	80	80	TBD	mA	
IDD7	1400	1840	TBD	mA	

M378B5673EH1 : 2GB(256Mx64) Module

Symbol	CF8 (DDR3-1066@CL=7)	CH9 (DDR3-1333@CL=9)	CK0 (DDR3-1600@CL=11)	Unit	Notes
IDD0	720	800	TBD	mA	
IDD1	840	920	TBD	mA	
IDD2P0(slow exit)	160	160	TBD	mA	
IDD2P1(fast exit)	400	400	TBD	mA	
IDD2N	480	560	TBD	mA	
IDD2Q	480	560	TBD	mA	
IDD3P(fast exit)	400	400	TBD	mA	
IDD3N	600	680	TBD	mA	
IDD4R	1080	1280	TBD	mA	
IDD4W	1160	1360	TBD	mA	
IDD5B	1440	1560	TBD	mA	
IDD6	160	160	TBD	mA	
IDD7	1640	2120	TBD	mA	

M391B2873EH1: 1GB(128Mx72) Module

Symbol	CF8 (DDR3-1066@CL=7)	CH9 (DDR3-1333@CL=9)	CK0 (DDR3-1600@CL=11)	Unit	Notes
IDD0	540	585	TBD	mA	
IDD1	675	720	TBD	mA	
IDD2P0(slow exit)	90	90	TBD	mA	
IDD2P1(fast exit)	225	225	TBD	mA	
IDD2N	270	315	TBD	mA	
IDD2Q	270	315	TBD	mA	
IDD3P(fast exit)	225	225	TBD	mA	
IDD3N	405	450	TBD	mA	
IDD4R	945	1125	TBD	mA	
IDD4W	1035	1215	TBD	mA	
IDD5B	1350	1440	TBD	mA	
IDD6	90	90	TBD	mA	
IDD7	1575	2070	TBD	mA	

M391B5673EH1: 2GB(256Mx72) Module

Symbol	CF8 (DDR3-1066@CL=7)	CH9 (DDR3-1333@CL=9)	CK0 (DDR3-1600@CL=11)	Unit	Notes
IDD0	810	900	TBD	mA	
IDD1	945	1035	TBD	mA	
IDD2P0(slow exit)	180	180	TBD	mA	
IDD2P1(fast exit)	450	450	TBD	mA	
IDD2N	540	630	TBD	mA	
IDD2Q	540	630	TBD	mA	
IDD3P(fast exit)	450	450	TBD	mA	
IDD3N	675	765	TBD	mA	
IDD4R	1215	1440	TBD	mA	
IDD4W	1305	1530	TBD	mA	
IDD5B	1620	1755	TBD	mA	
IDD6	180	180	TBD	mA	
IDD7	1845	2385	TBD	mA	

15.0 Input/Output Capacitance

15.1 Non ECC UDIMM

Parameter	Symbol	M378B2873EH1						Units	Notes
		DDR3-1066		DDR3-1333		DDR3-1600			
		Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	-	TBD	-	TBD	-	TBD	pF	
Input capacitance (CK and $\overline{CK}$)	CCK	-	TBD	-	TBD	-	TBD	pF	
Input capacitance (All other input-only pins)	CI	-	TBD	-	TBD	-	TBD	pF	
Input/output capacitance of ZQ pin	CZQ	-	TBD	-	TBD	-	TBD	pF	

Parameter	Symbol	M378B5673EH1				Units	Notes
		DDR3-1066		DDR3-1333			
		Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	-	TBD	-	TBD	pF	
Input capacitance (CK and $\overline{CK}$)	CCK	-	TBD	-	TBD	pF	
Input capacitance (All other input-only pins)	CI	-	TBD	-	TBD	pF	
Input/output capacitance of ZQ pin	CZQ	-	TBD	-	TBD	pF	

15.2 ECC UDIMM

Parameter	Symbol	M391B2873EH1				Units	Notes
		DDR3-1066		DDR3-1333			
		Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	-	TBD	-	TBD	pF	
Input capacitance (CK and $\overline{CK}$)	CCK	-	TBD	-	TBD	pF	
Input capacitance (All other input-only pins)	CI	-	TBD	-	TBD	pF	
Input/output capacitance of ZQ pin	CZQ	-	TBD	-	TBD	pF	

Parameter	Symbol	M391B5673EH1				Units	Notes
		DDR3-1066		DDR3-1333			
		Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	-	TBD	-	TBD	pF	
Input capacitance (CK and $\overline{CK}$)	CCK	-	TBD	-	TBD	pF	
Input capacitance (All other input-only pins)	CI	-	TBD	-	TBD	pF	
Input/output capacitance of ZQ pin	CZQ	-	TBD	-	TBD	pF	

16.0 Electrical Characteristics and AC timing

(0 °C<T_{CASE} ≤95 °C, V_{DDQ} = 1.5V ± 0.075V; V_{DD} = 1.5V ± 0.075V)

16.1 Refresh Parameters by Device Density

Parameter	Symbol		1Gb	2Gb	4Gb	8Gb	Units	Note
All Bank Refresh to active/refresh cmd time	tRFC		110	160	300	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	µs	
		85 °C < T_{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	µs	1

Note :

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

16.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR3-1066	DDR3-1333	DDR3-1600	Units	Note
Bin (CL - tRCD - tRP)	7-7-7	9-9-9	11-11-11		
Parameter	min	min	min		
CL	7	9	11	tCK	
tRCD	13.13	13.5	13.75	ns	
tRP	13.13	13.5	13.75	ns	
tRAS	37.5	36	35	ns	
tRC	50.63	49.5	48.75	ns	
tRRD	7.5	6.0	6.0	ns	
tFAW	37.5	30	30	ns	

16.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin

DDR3 SDRAM Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3-1066 Speed Bins

Speed			DDR3-1066		Units	Note
CL-nRCD-nRP			7 - 7 - 7			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	13.125	20	ns	
ACT to internal read or write delay time		tRCD	13.125	-	ns	
PRE command period		tRP	13.125	-	ns	
ACT to ACT or REF command period		tRC	50.625	-	ns	
ACT to PRE command period		tRAS	37.5	9*tREFI	ns	8
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,6
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3
Supported CL Settings			6,7,8		nCK	
Supported CWL Settings			5,6		nCK	

DDR3-1333 Speed Bins

Speed			DDR3-1333		Units	Note
CL-nRCD-nRP			9 -9 - 9			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	13.5 (13.125)[5,9]	20	ns	
ACT to internal read or write delay time		tRCD	13.5 (13.125)[5,9]	-	ns	
PRE command period		tRP	13.5 (13.125)[5,9]	-	ns	
ACT to ACT or REF command period		tRC	49.5 (49.125)[5,9]	-	ns	
ACT to PRE command period		tRAS	36	9*tREFI	ns	8
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,7
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 7	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,7
			(Optional) Note 5,9			
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			6,7,8,9		nCK	
Supported CWL Settings			5,6,7		nCK	

DDR3-1600 Speed Bins

Speed			DDR3-1600		Units	Note
CL-nRCD-nRP			11-11-11			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	13.75 (13.125)[5,9]	20	ns	
ACT to internal read or write delay time		tRCD	13.75 (13.125)[5,9]	-	ns	
PRE command period		tRP	13.75 (13.125)[5,9]	-	ns	
ACT to ACT or REF command period		tRC	48.75 (48.125)[5,9]	-	ns	
ACT to PRE command period		tRAS	35	9*tREFI	ns	
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,8
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 7, 8	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,8
			(Optional) Note 5,9			
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 8	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,8
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,8
			(Optional) Note 9,10			
	CWL = 8	tCK(AVG)	TBD		ns	1,2,3,4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,8
			(Optional) Note 9,10			
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 11	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	<1.5	ns	1,2,3,5
Supported CL Settings			6,7,8,9,10,11		nCK	
Supported CWL Settings			5,6,7,8		nCK	

16.3.1 Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

Note :

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next "SupportedCL".
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. "Reserved" settings are not allowed. User must program a different value.
5. "Optional" settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/ or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333(CL9) devices supporting downshift to DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin=36ns+13.125ns) for DDR3-1333(CL9) and 48.125ns (tRASmin+tRPmin=35ns+13.125ns) for DDR3-1600(CL11).

17.0 Timing Parameters by Speed Grade

Speed		DDR3-1066		DDR3-1333		DDR3-1600		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table						ps	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-90	90	-80	80	-70	70	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-80	80	-70	70	-60	60	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	180		160		140		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	160		140		120		ps	
Cumulative error across 2 cycles	tERR(2per)	- 132	132	- 118	118	-103	103	ps	
Cumulative error across 3 cycles	tERR(3per)	- 157	157	- 140	140	-122	122	ps	
Cumulative error across 4 cycles	tERR(4per)	- 175	175	- 155	155	-136	136	ps	
Cumulative error across 5 cycles	tERR(5per)	- 188	188	- 168	168	-147	147	ps	
Cumulative error across 6 cycles	tERR(6per)	- 200	200	- 177	177	-155	155	ps	
Cumulative error across 7 cycles	tERR(7per)	- 209	209	- 186	186	-163	163	ps	
Cumulative error across 8 cycles	tERR(8per)	- 217	217	- 193	193	-169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	- 224	224	- 200	200	-175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	- 231	231	- 205	205	-180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	- 237	237	- 210	210	-184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	- 242	242	- 215	215	-188	188	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max						ps	24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26
Data Timing									
DQS,$\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-600	300	-500	250	-450	225	ps	13,14, f
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	300	-	250	-	225	ps	13,14, f
Data setup time to DQS, $\overline{DQS}$ referenced to V_{IH}(AC)V_{IL}(AC) levels	tDS(base)	25	-	30	-	10		ps	d, 17
Data hold time to DQS, $\overline{DQS}$ referenced to V_{IH}(AC)V_{IL}(AC) levels	tDH(base)	100	-	65	-	45		ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	490	-	400	-	360		ps	28
Data Strobe Timing									
DQS, $\overline{DQS}$ READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	tCK	13, 19, g
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	tCK	11, 13, b
DQS, $\overline{DQS}$ output high time	tQSH	0.38	-	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{DQS}$ output low time	tQSL	0.38	-	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{DQS}$ WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	
DQS, $\overline{DQS}$ WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK	
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	tDQSCK	-300	300	-255	255	-225	225	ps	13,f
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-600	300	-500	250	-450	225	ps	13,14,f
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	300	-	250	-	225	ps	12,13,14
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	29, 31
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30, 31
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.27	0.27	tCK(avg)	c
DQS,$\overline{DQS}$ faling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	0.2	-	0.18	-	tCK(avg)	c, 32
DQS,$\overline{DQS}$ faling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.2	-	0.2	-	0.18	-	tCK(avg)	c, 32

Speed		DDR3-1066		DDR3-1333		DDR3-1600		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-	max (12nCK,15ns)	-		
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See 13.3 " Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin" on page 37						ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,7.5ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e
Four activate window for 1KB page size	tFAW	37.5	-	30	-	30	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	45	-	40	-	ns	e
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{IH}(AC) / V_{IL}(AC) levels	tIS(base)	125	-	65	-	TBD	-	ps	b,16
Command and Address hold time from CK, $\overline{CK}$ referenced to V_{IH}(AC) / V_{IL}(AC) levels	tIH(base)	200	-	140	-	TBD	-	ps	b,16
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{IH}(AC) / V_{IL}(AC) levels	tIS(base) AC150	125 + 150	-	65+125	-	TBD+125	-	ps	b,16,27
Control & Address Input pulse width for each input	tIPW	780	-	620	-	560	-	ps	28
Calibration Timing									
Power-up and RESET calibration time	tZQinitl	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK	
Normal operation short calibration time	tZQCS	64	-	64	-	64	-	nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC+ 10ns)	-	max(5nCK,tRFC+ 10ns)	-	max(5nCK,tRFC+ 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		

Speed		DDR3-1066		DDR3-1333		DDR3-1600		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Percharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK,6ns)	-	max (3nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-	max (3nCK,5ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK	10
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-		20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timing									
ODT high time without write command or with wirte command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns	
ODT turn-on	tAON	-300	300	-250	250	-225	225	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing									
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK	3
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK	3
Setup time for tDQSS latch	tWLS	245	-	195	-	165	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	tWLH	245	-	195	-	165	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

17.1 Jitter Notes

Specific Note a Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.

Specific Note b These parameters are measured from a command/address signal (CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c These parameters are measured from a data strobe signal (DQS(L/U), $\overline{\text{DQS}}$(L/U)) crossing to its respective clock signal (CK, $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{\text{DQS}}$(L/U)) crossing.

Specific Note e For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

Specific Note f When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

Specific Note g When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

17.2 Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON see "Device Operation"
8. For definition of RTT turn-off time tAOF see "Device Operation".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Device Operation Datasheet
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is valid for RON34
14. Single ended signal parameter.
15. tREFI depends on T_{OPER}
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate, Note for DQ and DM signals, V_{REF}(DC) = V_{REF}DQ(DC). FOr input only pins except RESET, V_{REF}(DC)=V_{REF}CA(DC).
    See "Address/ Command Setup, Hold and Derating"
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, V_{REF}(DC)= V_{REF}DQ(DC). For input only pins except $\overline{RESET}$, V_{REF}(DC)=V_{REF}CA(DC).
    See "Data Setup, Hold and Slew Rate Derating".
18. Start of internal write transaction is definited as follows ;
    For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
    For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
    For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side. See "Device Operation"
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Altough CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation".
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens x Tdriftrate}) + (\text{VSens x Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% /°C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

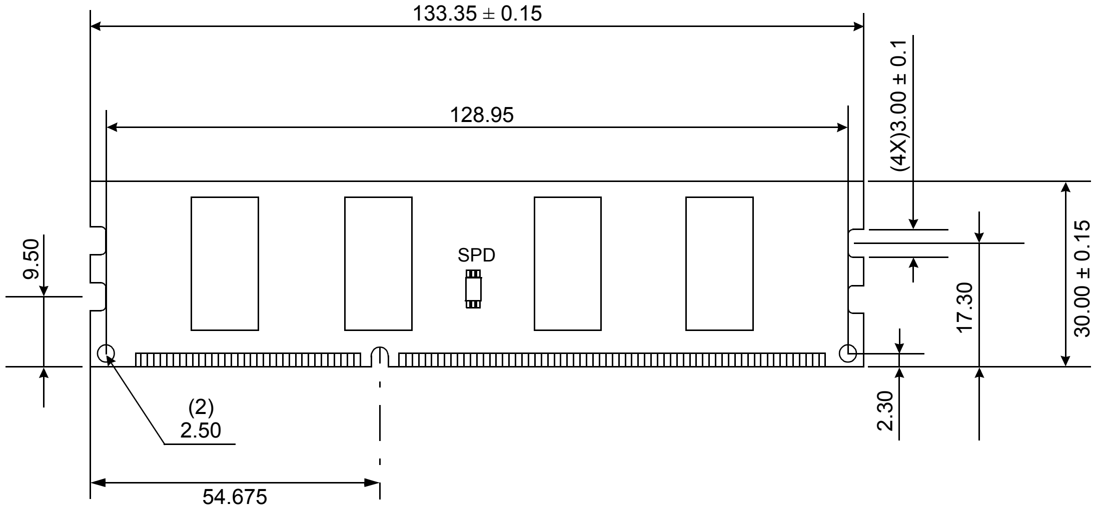
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

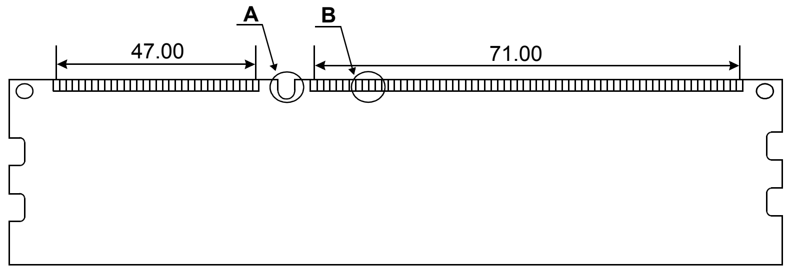
24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of V_{REF}(DC) and the consecutive crossing of V_{REF}(DC)
29. tDQSL describes the instantaneous differential input low pulse width on DQS-$\overline{DQS}$, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS-$\overline{DQS}$, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
32. tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

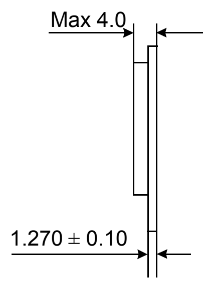
18.0 Physical Dimensions

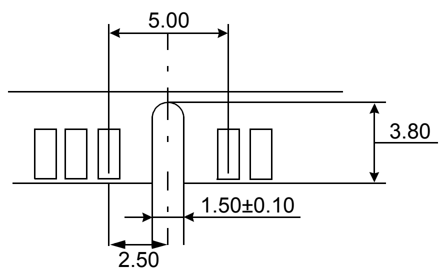
18.1 64Mbx16 based 64Mx64 Module (1 Rank)

Units : Millimeters

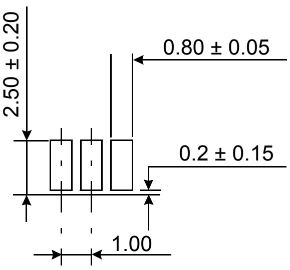




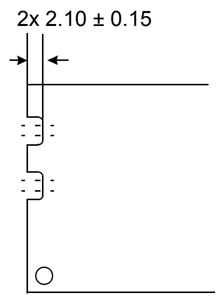




Detail A



Detail B

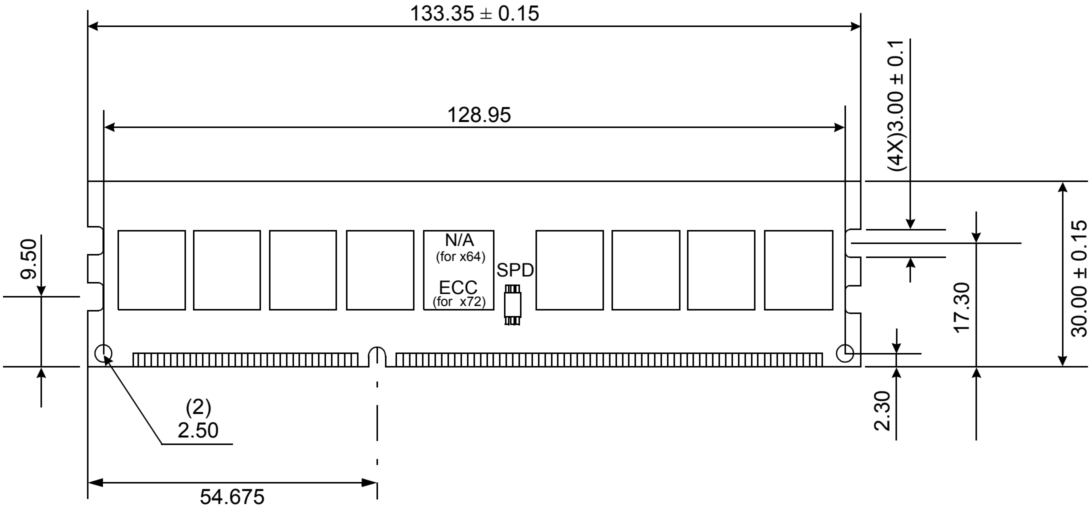


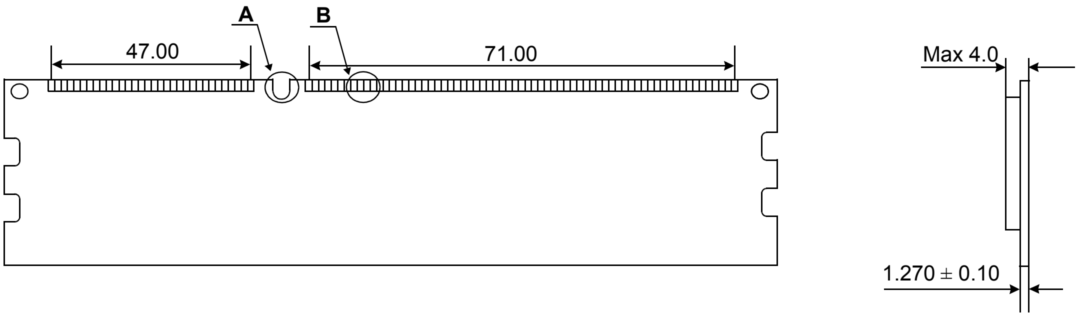
The used device is 64M x16 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B1G1646E-HC**

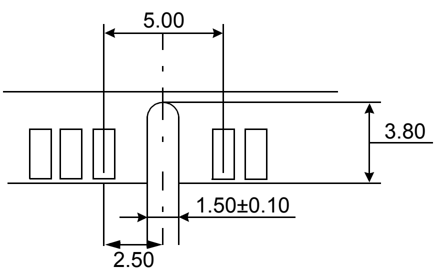
* Note : Tolerances on all dimensions ±0.15 unless otherwise specified.

18.2 128Mbx8 based 128Mx64/x72 Module (1 Rank)

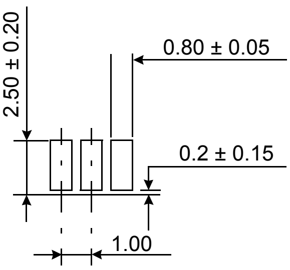
Units : Millimeters



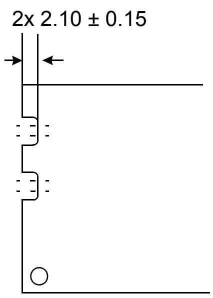




Detail A



Detail B

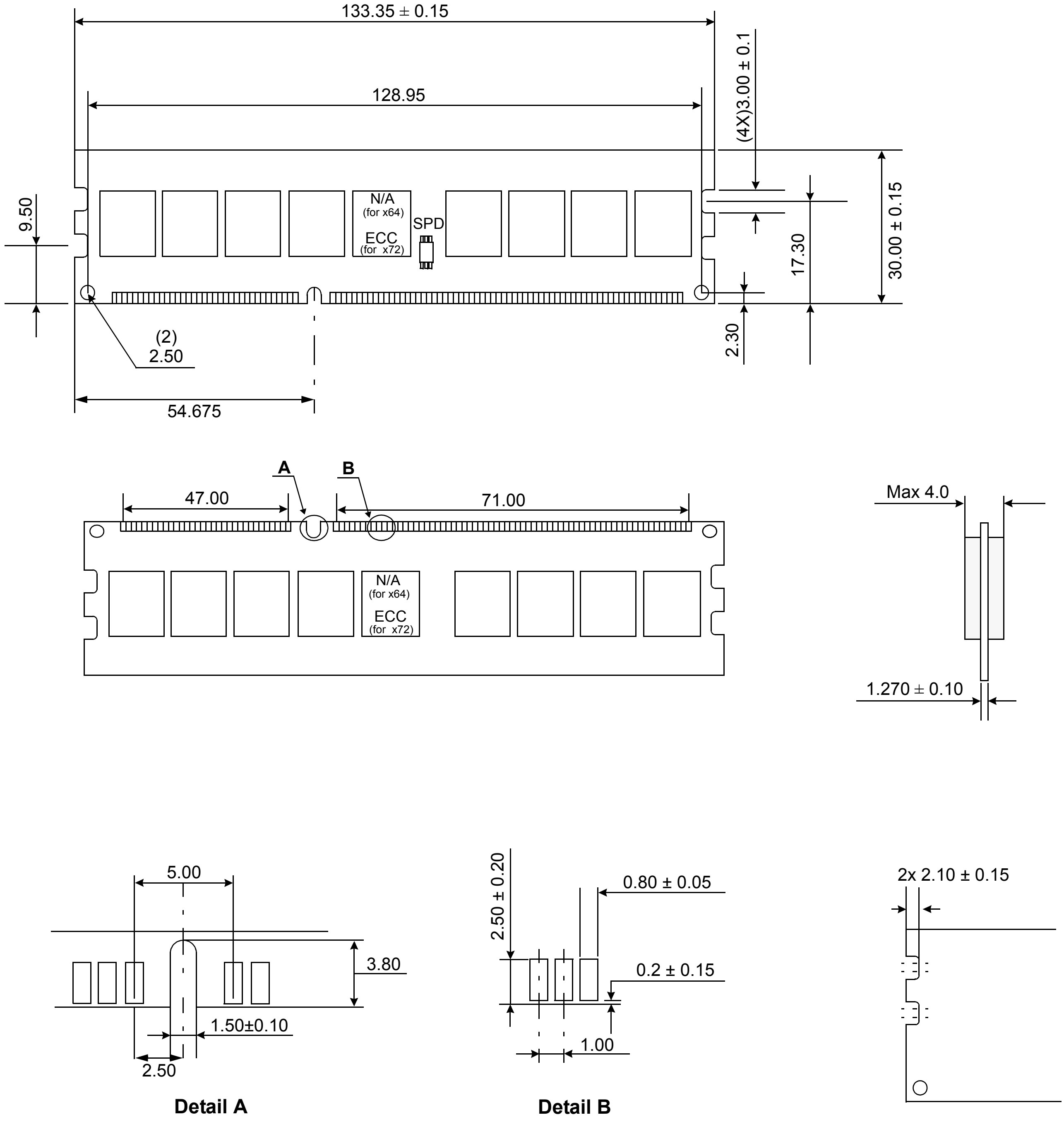


The used device is 128M x8 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B1G0846E-HC**

* Note : Tolerances on all dimensions ±0.15 unless otherwise specified.

18.3 128Mbx8 based 256Mx64/x72 Module (2 Ranks)

Units : Millimeters



The used device is 128M x8 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B1G0846E-HC**

* Note : Tolerances on all dimensions ±0.15 unless otherwise specified.